Remarks

Claims 1-4 and 6-12 have been examined. The Examiner has rejected claims 1-4 and 6-12. By this amendment, claims 1-4 and claims 6-12 are amended. Thus, claims 1-4 and 6-12 remain in this application.

Applicant has reviewed the examiner's response to the amendment, and response to arguments, and appreciates the examiner withdrawing his objections and rejections specified in the first office action.

Claim Objections

The examiner objected to claim 7 because he could not determine "whether the set of queues is referring to the same one queue or not". Applicant has amended claim 7 to better clarify the invention.

The examiner objected to claim 12 because it was unclear with respect to "two memory ports" and therefore read execution unit to mean "two memory units". Applicant has amended claim 12 to better clarify the invention.

Claim Rejections - 35 USC §112

The Examiner rejected claims 7-12 under 35 USC §112, second paragraph, as being indefinite. The examiner further indicated that there was no antecedent basis for the limitation "the instruction source" in claim 7. Applicant has amended claims 7-12 to clearly and distinctly claim the invention.

Claim Rejections - 35 USC §102

The examiner rejected claim 1, 7, 11-12 under 35 USC §102 as being anticipated by Parady (U.S. Patent No. 5,933,627). Applicant respectfully traverses. But, before providing a claim by claim analysis, applicant believes that a brief overview of Parady and applicant's invention would be helpful.

Parady describes a method and apparatus for switching between threads of a program in response to a long-latency event. (see Abstract). More specifically, Parady shows, in Figure 3, a decode unit 14 which is connected to four instruction buffers 102, 104, 106, 108 (supporting four instruction threads), which are connected to a dispatch unit 28. see

Col. 3, lines 37-42. The dispatch unit 28 then provides four decoded instructions at a time to one of eight functional units 32-46. see Col. 3, lines 13-18. What applicant would appreciate the examiner understanding, at this point, is that Parady only fetches instructions for one instruction stream at a time from the instruction cache 12. That is, Parady's decode unit 14 fetches 4 instructions for a first instruction stream. Then, by using either a round-robin counter 128, or based on an L2 cache miss 114, thread switching logic 112 causes the decode unit 14 to fetch four instructions for another instruction thread. see Col. 3, line 50 thru Col. 4 line 12. Thus, Parady teaches a single connection between the instruction cache 12 and the decode unit 14 for fetching "instructions *from a particular thread*" for the dispatch unit 28. see Col. 3 lines 39-42. Parady does not fetch instructions for multiple threads. Furthermore, Parady fetches the same number of instructions at one time (i.e., 4), for placement into the instruction buffer 26, as are dispatched by the dispatch unit 28 (i.e., 4). Please see Figure 1 where 4 instructions are shown to flow on a single bus from the instruction cache 12 to the decode unit 14, from the decode unit 14 to the instruction buffer 26, from the instruction buffer 26 to the dispatch unit 28, and from the dispatch unit 28 to the eight functional units 32-46. Thus, in Parady, there is a direct association with the number of instructions fetched, queued, and dispatched.

In contrast to Parady, applicant specifically shows multiple connections between the fetch unit 33 and the instruction cache 31. In one embodiment, each of these connections is capable of fetching eight instructions from the instruction cache. Thus, the fetch unit 33 of applicant's invention is fetching instructions for multiple instruction streams at the same time. Further, the choice of which ones of the instruction streams are fetched is controlled by select logic 35, not in some round-robin fashion, but rather, based on the contents of the instruction queues 39. As mentioned in the specification, the selection logic 35 monitors the state of each queue in set 39, and determines two threads from which to fetch instructions in a particular cycle. see page 6, lines 21-29. This concept of allowing a larger pool of instructions after the dispatch stage to control, at least in part, the fetching of instructions for a smaller number of streams is novel, and is what the present invention is directed to. Further, applicant's invention disassociates the fetching of multiple streams from dispatch, to essentially decouple the fetching apparatus from the

dispatch. And, the number of instructions fetched at one time (16, 8 for two streams) is greater than the number of instructions dispatched. This insures that the instruction queues are always full across all of the streams.

With the above in mind, claim 1 is repeated below, as amended, for ease of reference:

1. (Currently amended) A pipelined multistreaming processor, comprising:

an instruction cache;

fetch logic coupled to said instruction cache enabled to concurrently fetch instructions for a plurality of instruction streams from the instruction cache;

a plurality of instruction queues coupled to said fetch logic where each one of said plurality of instruction queues is associated with at least one of said plurality of instruction streams;

a dispatch stage coupled to said plurality of instruction queues for selecting and dispatching instructions for said plurality of instruction streams to a set of execution units; and

select logic coupled to said instruction cache for selecting ones of said plurality of instruction streams to fetch instructions from said instruction cache.

With respect to claim 1, the examiner indicated that Parady taught the invention as claimed. In view of the foregoing amendment to claim 1, applicant believes that the rejection based on Parady is moot. Claim 1, as amended, particularly recites fetch logic enabled to concurrently fetch instructions for a plurality of instruction streams. As stated above, this is nowhere taught, suggested, or even hinted at by Parady. Parady fetches four instructions at a time, for a single instruction stream. In contrast, applicant claims and his invention teaches fetching instructions for a plurality of instruction streams, concurrently. Furthermore, claim 1 recites select logic, which selects from the plurality of instruction streams, ones of the streams for fetching. Parady, in contrast selects merely one instruction stream for fetching. Applicant claims, and teaches, the novel aspect of concurrently fetching instructions for a plurality of streams, and in one embodiment (as recited in claim 2), for fetching instructions for a plurality of streams where the number

of streams fetched is less than the number of executing instruction streams. Applicant respectfully submits that such teaching is nowhere present in Parady. For these reasons, applicant respectfully requests the examiner to withdraw his rejection of claim 1.

With respect to claim 7, it is repeated below, as amended, for ease of reference:

7. In a multistreaming processor, the processor executing a plurality of instruction streams, a method for decoupling fetching of instructions for the plurality of instruction streams from the dispatch of those instructions for execution, the method comprising:

placing a plurality of instruction queues in the processor, one instruction queue for each instruction stream, the plurality of queues located between fetch logic, which fetches instructions for the instruction streams, and dispatch logic, which dispatches instructions for the instruction streams; and.

placing select logic in the processor, the select logic selecting a plurality of instruction streams for which to fetch instructions from an instruction cache, the number of instruction streams selected by the select logic being less than the number of instruction streams in the processor;

wherein by selecting a plurality of instruction streams for fetching which is less than the number of instruction streams executing, the association between fetching of instructions, and their dispatch is effectively decoupled.

In view of the amendment to claim 7, applicant submits that the examiner's rejection is now moot. Applicant submits that, similarly to claim 1, claim 7 particularly recites select logic "selecting a plurality of instruction streams for which to fetch instructions". As mentioned above, Parady teaches fetching for one instruction stream at a time. Nowhere does Parady teach, suggest, or even hint at fetching for a plurality of instruction streams, much less fetching for a plurality of instruction streams, the number of streams fetched being less than the number of streams executing, to thereby decouple the fetching of instruction streams from their dispatch. For these reasons, and for those stated above with respect to claim 1, applicant respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claims 11 and 12, these have been amended, and depend from claim 7 and add further limitations which are neither anticipated nor obviated by Parady. For the reasons stated above, applicant respectfully requests the examiner to withdraw his rejection of these claims.

Claim Rejections - 35 USC §103

The examiner rejected claims 2-4 and 8 under 35 USC §103(a) as being unpatentable over Parady in view of Emer (6,470,443). More specifically, the examiner indicated that Emer taught "the number of streams in the plurality of streams is eight, and the number of streams selected for which to fetch instructions in each cycle is two." referencing Figures 8A and 8B and column 12, line 22 to column 13, line 60. The Examiner indicated that it would have been obvious to one of ordinary skill in the art to modify the design of Parady to incorporate the thread selection and instruction fetching mechanism of Emer so that multiple instructions may be fetched in a single cycle. Applicant respectfully traverses.

Applicant has already discussed Parady at length, and reiterates per the above Parady's lack of teaching with respect to Applicant's invention as claimed. Further, applicant suggests that the Examiner has taken Emer's teaching of fetching of multiple streams, and combined this with the teaching of Parady without explaining the motivation to combine Parady with Emer. There is no hint or suggestion in Parady to combine his invention with a device such as Emer (to fetch multiple streams), nor is there any teaching, hint or suggestion in Emer to combine his multiple stream fetching mechanism with the teachings of Parady. As the Federal Circuit has held, "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992), at 1783-1784. Applicant respectfully submits that there is nothing in either Parady nor Emer to suggest the combination. Applicant therefore respectfully requests the Examiner to withdraw his rejection of these claims.

The Examiner further rejected claims 6 and 12 under 35 USC §103(a) as being unpatentable over Parady. In view of the foregoing amendments, and for the foregoing

arguments, applicant respectfully submits that these claims are neither anticipated nor obviated by Parady. Applicant therefore respectfully requests the examiner to withdraw his rejection of these claims.

For all of the above reasons, applicant respectfully requests the examiner to withdraw his rejection of all of the remaining claims, and that a timely Notice of Allowance be issued in this case.

Applicant earnestly requests the examiner to telephone him at the direct dial number printed below if the examiner has any questions or suggestions concerning the application.

Respectfully submitted,

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